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EXAMINER	
LI, AIMEE J	

ART UNIT	PAPER NUMBER
2183	19

DATE MAILED: 06/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/505,949	CHOW ET AL.	
	Examiner	Art Unit	
	Aimee J Li	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. In view of the Appeal Brief filed on 13 April 2004, PROSECUTION IS HEREBY REOPENED. A new grounds of rejection is set forth below.

2. To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) request reinstatement of the appeal.

3. If reinstatement of the appeal is requested, such request must be accompanied by a supplemental appeal brief, but no new amendments, affidavits (37 CFR 1.130, 1.131 or 1.132) or other evidence are permitted. See 37 CFR 1.193(b)(2).

4. Claims 1-19 have been considered.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claim 5 recites the limitation "the token" in line 2. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claim10 and 14 rejected under 35 U.S.C. 102(b) as being taught by Loper et al., U.S. Patent Number 5,611,063 (herein referred to as Loper).

9. Referring to claim 10, Loper has taught a method in a processor comprising:

a. Fetching an input from at least one of a plurality of floating-point registers; detecting whether the input includes a token (Applicant's claim 10) (Loper column 3, lines 21-51);

b. If the token is detected in the input, checking what mode the processor is in (Applicant's claim 10) (Loper column 1, lines 10-22; column 1, line 65 to column 2, line 23; column 5, line 6 to column 6, line 35; and Figure 3);

c. If the processor is in a first mode, processing the input to render an arithmetic result (Applicant's claim 10) (Loper column 1, lines 10-22; column 1, line 65 to column 2, line 23; column 3, lines 21-51; column 5, line 6 to column 6, line 35; and Figure 3);

d. If the processor is in a second mode, performing a token specific operation (Applicant's claim 10) (Loper column 1, lines 10-22; column 1, line 65 to column 2, line 23; column 5, line 6 to column 6, line 35; and Figure 3); and

e. Producing an output (Applicant's claim 10) (Loper column 1, lines 10-22; column 1, line 65 to column 2, line 23; column 5, line 6 to column 6, line 35; and Figure 3).

10. Referring to claim 14, Loper has taught wherein the token represents a "not a thing value" (NaTVal) that defines an unsuccessful speculative load request (Loper column 1, lines 10-22; column 1, line 65 to column 2, line 23; column 5, line 6 to column 6, line 35; and Figure 3).

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claims 1-2, 4-5, 7-13 and 15-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mohammed, U.S. Patent Number 6,366,998 (herein referred to as Mohammed) in view of Blomgren, U.S. Patent Number 5,685,009 (herein referred to as Blomgren).

13. Referring to claim 1, Mohammed has taught a processor comprising:

a. A first instruction set engine to process instructions from a first instruction set architecture (ISA) having a first word size (Mohammed column 4, lines 28-47; column 5, line 39 to column 6, line 34; column 8, line 35-63; column 9, lines 37-44; and Figures 1-8);

b. A second instruction set engine to process instructions from a second ISA having a second word size, the second word size being different than the first word size (Mohammed column 4, lines 28-47; column 5, line 39 to column 6, line 34; column 8, line 35-63; column 9, lines 37-44; and Figures 1-8);

c. A mode identifier (Mohammed column 4, lines 28-47; column 5, line 39 to column 6, line 34; column 8, line 13-63; column 9, lines 37-44; and Figures 1-8);

d. A plurality of registers shared by the first instruction set engine and the second instruction set engine (Mohammed column 5, line 39-51; column 9, lines 15-36; and Figures 2 and 10); and

e. A floating-point unit coupled to the registers, the floating-point unit processing an input responsive to the mode identifier to produce an output (Mohammed column 5, line 39-51; column 8, line 35-63; column 9, lines 37-44; and Figures 2 and 8).

14. Mohammed has not explicitly taught floating-point registers. However, Mohammed has taught that any type of register file may be used in his system, and his example of scalar and vector register files are only examples (Mohammed column 9, lines 29-31). Blomgren has taught shared floating-point registers (Blomgren column 3, lines 5-22; column 17, lines 61-67; and column 18, lines 6-9). A person of ordinary skill in the art at the time the invention was made would have recognized that using floating-point registers store are wider in order to be compatible with the larger floating point data. Also, a person of ordinary skill in the art at the time the invention was made would have recognized that sharing the floating-point registers only requires the system to supply one set of floating-point registers, thereby shrinking the size and cost of the processor, and increases the efficiency of the processor by allowing the data to be explicitly addressed as opposed to transfer data from one register set to another before addressing the data. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use the shared floating-point registers of Blomgren in the device of Mohammed to increase compatibility between data types, decrease size and cost of the processor, and increase processor efficiency.

15. Referring to claim 2, Mohammed has not explicitly taught wherein the mode identifier is one of a plurality of bits in a processor status register. However, Mohammed has taught the functional units are reconfigurable and change modes depending upon the instruction received (Mohammed column 8, lines 13-34). Blomgren has taught wherein the mode identifier is one of a plurality of bits in a processor status register (Blomgren column 4, lines 63-65 and column 20, lines 18-30). A person of ordinary skill in the art at the time the invention was made would have recognized that storing the mode identifier in a processor status register would ensure that the data was correctly executed and the resultant data would not be erroneous. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the processor statue register of Blomgren in the device of Mohammed to avoid erroneous resultant data.

16. Referring to claims 4-5 and 7, Mohammed has taught

a. Wherein the input includes data stored in at least one of the registers (Applicant's claim 4) (Mohammed column 4, lines 28-47; column 5, line 39 to column 6, line 34; column 8, line 35-63; column 9, lines 37-44; and Figure 2).

17. Mohammed has not explicitly taught:

a. Floating-point registers (Applicant's claim 4);

b. Wherein the input may contain a token, wherein the floating-point registers are 82 bits wide, and wherein the token being an 82 bit processor known value (Applicant's claim 5);

c. Wherein the floating point registers each comprise (Applicant's claim 7):

i. A sign bit (Applicant's claim 7);

ii. An exponent (Applicant's claim 7); and

iii. A significand (Applicant's claim 7).

18. However, Mohammed has taught that any type of register file may be used in his system, and his example of scalar and vector register files are only examples (Mohammed column 9, lines 29-31). Blomgren has taught

a. Shared floating-point registers (Applicant's claim 4) (Blomgren column 3, lines 5-22; column 17, lines 61-67; and column 18, lines 6-9). ;

b. Wherein the input may contain a token, wherein the floating-point registers are 82 bits wide, and wherein the token being an 82 bit processor known value (Applicant's claim 5) (Blomgren column 18, lines 34-65 and column 20, lines 26-30). In regards to Blomgren, the data stored in the floating point registers is 82 bits wide, which includes the token stored in the floating point registers.

c. Wherein the floating point registers each comprise (Applicant's claim 7):

i. A sign bit (Applicant's claim 7) (Blomgren column 2, lines 12-22). In regards to Blomgren, it is inherent that the significand, also known as the mantissa, includes the sign bit. Please see FOLDOC definition mantissa ©1996.

ii. An exponent (Applicant's claim 7) (Blomgren column 2, lines 12-22); and

iii. A significand (Applicant's claim 7) (Blomgren column 2, lines 12-22). In regards to Blomgren, it is inherent and well-known in the art that a significand is the same as the mantissa. Please see David Goldberg's "What Every Computer Scientist Should Know About Floating-Point

Arithmetic" ©1991, specifically under the section titled "Floating-point Formats", paragraph 2 "where *d.dd... d* is called the *significand*[2]" which refers to footnote 2 which says "This term was introduced by Forsythe and Moler [1967], and has generally replaced the older term *mantissa*.

19. A person of ordinary skill in the art at the time the invention was made would have recognized that using floating-point registers store are wider in order to be compatible with the larger floating point data. Also, a person of ordinary skill in the art at the time the invention was made would have recognized that sharing the floating-point registers only requires the system to supply one set of floating-point registers, thereby shrinking the size and cost of the processor, and increases the efficiency of the processor by allowing the data to be explicitly addressed as opposed to transfer data from one register set to another before addressing the data. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use the shared floating-point registers of Blomgren in the device of Mohammed to increase compatibility between data types, decrease size and cost of the processor, and increase processor efficiency.

20. Referring to claim 8, Mohammed has taught wherein the mode identifier indicates whether the processor is in a first mode or a second mode (Mohammed column 4, lines 28-47; column 5, line 39 to column 6, line 34; column 8, line 35-63; column 9, lines 37-44; and Figures 1-8).

21. Referring to claim 9, Mohammed has taught wherein the mode identifier indicates whether the processor is in a 32 bit word ISA mode or a 64 bit word ISA mode (Mohammed

column 5, lines 52-56). In regards to Mohammed, 32 bit words and 64 bit words are multiples of 8, specifically 32 is 4 multiples of 8 and 64 is 8 multiples of 8.

22. Referring to claim 10, Mohammed has taught a method in a processor comprising:

a. Fetching an input from at least one of a plurality of registers (Mohammed column 4, lines 28-47; column 5, line 39 to column 6, line 34; column 8, line 35-63; column 9, lines 37-44; and Figures 1-8);

b. Detecting whether the input includes a token (Mohammed column 4, lines 28-47; column 5, line 39 to column 6, line 34; column 8, line 13-63; column 9, lines 37-44; and Figures 1-8);

c. If the token is detected in the input, checking what mode the processor is in (Mohammed column 8, lines 13-63);

d. If the processor is in a first mode, processing the input to render an arithmetic result (Mohammed column 4, lines 28-47; column 5, line 39 to column 6, line 34; column 8, line 35-63; column 9, lines 37-44; and Figures 1-8);

e. If the processor is in a second mode, performing a token specific operation (Mohammed column 4, lines 28-47; column 5, line 39 to column 6, line 34; column 8, line 35-63; column 9, lines 37-44; and Figures 1-8); and

f. Producing an output (Mohammed column 4, lines 28-47; column 5, line 39 to column 6, line 34; column 8, line 35-63; column 9, lines 37-44; and Figures 1-8).

23. Mohammed has not explicitly taught floating-point registers. However, Mohammed has taught that any type of register file may be used in his system, and his example of scalar and vector register files are only examples (Mohammed column 9, lines 29-31). Blomgren has

taught shared floating-point registers (Blomgren column 3, lines 5-22; column 17, lines 61-67; and column 18, lines 6-9). A person of ordinary skill in the art at the time the invention was made would have recognized that using floating-point registers store are wider in order to be compatible with the larger floating point data. Also, a person of ordinary skill in the art at the time the invention was made would have recognized that sharing the floating-point registers only requires the system to supply one set of floating-point registers, thereby shrinking the size and cost of the processor, and increases the efficiency of the processor by allowing the data to be explicitly addressed as opposed to transfer data from one register set to another before addressing the data. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use the shared floating-point registers of Blomgren in the device of Mohammed to increase compatibility between data types, decrease size and cost of the processor, and increase processor efficiency.

24. Referring to claim 11, Mohammed has taught wherein the input is comprised of at least one operand and at least one operator; wherein detecting comprises examining the at least one operand to determine whether any of the operands correspond to the token; and wherein checking comprises examining a mode identifier to determine whether the processor is in the first mode or the second mode (Mohammed column 4, lines 28-47; column 5, line 39 to column 6, line 34; column 8, line 13-63; column 9, lines 37-44; and Figures 1-8).

25. Referring to claim 12, Mohammed has taught wherein processing comprises executing at least one operation on the at least one operand according to the at least one operator to achieve a result (Mohammed column 4, lines 28-47; column 5, line 39 to column 6, line 34; column 8, line 13-63; column 9, lines 37-44; and Figures 1-8).

26. Referring to claim 13, Mohammed has taught wherein performing comprises propagating the token; and wherein producing output comprises setting the output to be the token (Mohammed column 4, lines 28-47; column 5, line 39 to column 6, line 34; column 8, line 13-63; column 9, lines 37-44; and Figures 1-8).

27. Referring to claim 15, Mohammed has taught wherein checking comprises checking a mode identifier (Mohammed column 4, lines 28-47; column 5, line 39 to column 6, line 34; column 8, line 13-63; column 9, lines 37-44; and Figures 1-8).

28. Referring to claim 16, Mohammed has not explicitly taught wherein checking comprises a mode identifier bit in a processor status register. However, Mohammed has taught the functional units are reconfigurable and change modes depending upon the instruction received (Mohammed column 8, lines 13-34). Blomgren has taught wherein checking comprises a mode identifier bit in a processor status register (Blomgren column 4, lines 63-65 and column 20, lines 18-30). A person of ordinary skill in the art at the time the invention was made would have recognized that storing the mode identifier in a processor status register would ensure that the data was correctly executed and the resultant data would not be erroneous. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the processor statue register of Blomgren in the device of Mohammed to avoid erroneous resultant data.

29. Referring to claim 17, Mohammed has taught wherein the first mode is a 32 bit word ISA mode and the second mode is a 64 bit word ISA mode (Mohammed column 5, lines 52-56). In regards to Mohammed, 32 bit words and 64 bit words are multiples of 8, specifically 32 is 4 multiples of 8 and 64 is 8 multiples of 8.

30. Referring to claim 18, Mohammed has taught a multi-mode processor comprising:

a. A plurality of instruction set engines to process instructions from a plurality of instruction set architectures having different word sizes (Mohammed column 4, lines 28-47; column 5, line 39 to column 6, line 34; column 8, line 35-63; column 9, lines 37-44; and Figures 1-8);

b. A mode identifier (Mohammed column 4, lines 28-47; column 5, line 39 to column 6, line 34; column 8, line 13-63; column 9, lines 37-44; and Figures 1-8);

c. A plurality of registers shared by the instruction set engines (Mohammed column 5, line 39-51; column 9, lines 15-36; and Figures 2 and 10); and

d. A floating-point unit coupled to the registers, the floating-point unit processing an input responsive to the mode identifier (Mohammed column 5, line 39-51; column 8, line 35-63; column 9, lines 37-44; and Figures 2 and 8).

31. Mohammed has not explicitly taught floating-point registers. However, Mohammed has taught that any type of register file may be used in his system, and his example of scalar and vector register files are only examples (Mohammed column 9, lines 29-31). Blomgren has taught shared floating-point registers (Blomgren column 3, lines 5-22; column 17, lines 61-67; and column 18, lines 6-9). A person of ordinary skill in the art at the time the invention was made would have recognized that using floating-point registers store are wider in order to be compatible with the larger floating point data. Also, a person of ordinary skill in the art at the time the invention was made would have recognized that sharing the floating-point registers only requires the system to supply one set of floating-point registers, thereby shrinking the size and cost of the processor, and increases the efficiency of the processor by allowing the data to be

explicitly addressed as opposed to transfer data from one register set to another before addressing the data. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use the shared floating-point registers of Blomgren in the device of Mohammed to increase compatibility between data types, decrease size and cost of the processor, and increase processor efficiency.

32. Referring to claim 19, Mohammed has taught a method in a multi-mode processor comprising:

a. Fetching an input from at least one of a plurality of registers (Mohammed column 4, lines 28-47; column 5, line 39 to column 6, line 34; column 8, line 35-63; column 9, lines 37-44; and Figures 1-8);

b. Detecting whether the input includes at least one token of a plurality of tokens (Mohammed column 4, lines 28-47; column 5, line 39 to column 6, line 34; column 8, line 13-63; column 9, lines 37-44; and Figures 1-8);

c. If at least one token is detected in the input, checking what mode the processor is in (Mohammed column 8, lines 13-63);

d. Processing the input to render an arithmetic result when the processor is in at least a first mode of a plurality of modes (Mohammed column 4, lines 28-47; column 5, line 39 to column 6, line 34; column 8, line 35-63; column 9, lines 37-44; and Figures 1-8);

e. Performing a token specific operation when the processor is in at least a second mode of a plurality of modes (Mohammed column 4, lines 28-47; column 5, line

39 to column 6, line 34; column 8, line 35-63; column 9, lines 37-44; and Figures 1-8).

33. Mohammed has not explicitly taught floating-point registers. However, Mohammed has taught that any type of register file may be used in his system, and his example of scalar and vector register files are only examples (Mohammed column 9, lines 29-31). Blomgren has taught shared floating-point registers (Blomgren column 3, lines 5-22; column 17, lines 61-67; and column 18, lines 6-9). A person of ordinary skill in the art at the time the invention was made would have recognized that using floating-point registers store are wider in order to be compatible with the larger floating point data. Also, a person of ordinary skill in the art at the time the invention was made would have recognized that sharing the floating-point registers only requires the system to supply one set of floating-point registers, thereby shrinking the size and cost of the processor, and increases the efficiency of the processor by allowing the data to be explicitly addressed as opposed to transfer data from one register set to another before addressing the data. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use the shared floating-point registers of Blomgren in the device of Mohammed to increase compatibility between data types, decrease size and cost of the processor, and increase processor efficiency.

34. Claims 3 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mohammed, U.S. Patent Number 6,366,998 (herein referred to as Mohammed) in view of Blomgren, U.S. Patent Number 5,685,009 (herein referred to as Blomgren) as applied to claim 1 above, and further in view of Loper et al., U.S. Patent Number 5,611,063 (herein referred to as Loper). Mohammed has taught an arithmetic unit responsive to the input and the mode identifier

(Applicant's claim 3) (Mohammed column 4, lines 28-47; column 5, line 39 to column 6, line 34; column 8, line 35-63; column 9, lines 37-44; and Figures 1-8).

35. Mohammed has not taught

a. Pre-processing hardware to detect if a token exists in the input (Applicant's claim 3);

b. Post-processing hardware to perform a token specific operation if a token exists in the input (Applicant's claim 3); and

c. Wherein the token represents a "not a thing value" (NaTVal) that defines an unsuccessful speculative load request (Applicant's claim 6).

36. Loper has taught

a. Pre-processing hardware to detect if a token exists in the input (Applicant's claim 3) (Loper column 1, lines 10-22; column 1, line 65 to column 2, line 23; column 5, line 6 to column 6, line 35; and Figure 3);

b. Post-processing hardware to perform a token specific operation if a token exists in the input (Applicant's claim 3) (Loper column 1, lines 10-22; column 1, line 65 to column 2, line 23; column 5, line 6 to column 6, line 35; and Figure 3);

c. Wherein the token represents a "not a thing value" (NaTVal) that defines an unsuccessful speculative load request (Applicant's claim 6) (Loper column 1, lines 10-22; column 1, line 65 to column 2, line 23; column 5, line 6 to column 6, line 35; and Figure 3).

37. A person of ordinary skill in the art at the time the invention was made would have recognized that speculative loads increase processor efficiency by speculatively executing

instructions based upon the speculative data, thereby ensuring the processor does not waste cycles in an idle state waiting for the instruction the load is dependent on, i.e. a branch instruction, to complete. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the speculative load of Loper in the device of Mohammed to increase processor efficiency.

Conclusion

38. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure as follows. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

a. Jaggar, U.S. Patent Number 5,568,646, has taught a multiple instruction set system

b. Blomgren et al., U.S. Patent Number 6,076,155, has taught a shared register set in a multiple instruction set system.

c. Cohen et al., U.S. Patent Number 5,781,457, has taught a multiple instruction set system.

39. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J Li whose telephone number is (703) 305-7596. The examiner can normally be reached on M-T 7:30am-5:00pm.

40. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

41. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AJL
Aimee J. Li
June 27, 2004

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100